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PATENT APPLICATION

STRUCTURE AND METHOD TO INCREASE DENSITY OF MIM CAPACITORS IN DAMASCENE PROCESSES

Inventor(s):

Subhas Bothra, a citizen of India, residing at
230 Prairie Dog Lane
Fremont, California 95049

Assignee:

ZEEVO, Inc.
2500 Condensa Avenue
Santa Clara, California 95051,
a corporation of Delaware

Entity: Small

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400

Structure and Method to Increase Density of MIM Capacitors in Damascene Processes

BACKGROUND OF THE INVENTION

The present invention is related to capacitor structures in integrated circuits and, in particular, to metal-insulator-metal capacitor structures in multilayer metal integrated circuits.

Current semiconductor processing technologies have enabled the reduction of sizes of transistors to critical dimensions below 0.25μm. Critical dimensions are now approaching 0.18μm and even more aggressive technologies are considering critical dimensions of 0.13μm. The operating frequencies of the resulting integrated circuits have risen to such an extent that MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) integrated circuits are being used for RF (Radio Frequency) applications. Such applications typically have analog and RF circuits which require passive elements, such as capacitors. In conventional MOS processes, including CMOS (Complementary Metal-Oxide-Semiconductor, the particular MOSFET technology of choice today), various capacitor structures, such as junction capacitors or gate capacitors, are available. However, these capacitor structures are voltage-dependent and do not meet the performance of a fixed capacitor, which is typically required in analog and RF circuits.

To satisfy this requirement, recent CMOS processes have provided MIM (metal-insulator-metal) capacitor structures which are implemented in the interconnect metallization layers of the integrated circuit. These multiple metallization layers are formed over the semiconductor substrate in which the source and drain regions of the transistors are defined to interconnect various elements of the integrated circuit. A single masking step can be added in the manufacturing process steps used to create conventional metal layers in the integrated circuit to create the capacitors. However, this results in very low density capacitors, i.e., capacitors with relatively low capacitance per unit area. Since the total area of a MIM capacitor can be a significant portion (15% – 30%) of the total substrate area of an integrated RF/Analog/Baseband integrated circuit and can be an even larger portion in a CMOS implementation of the radio section only of the integrated circuit, it is necessary to achieve as high an area density of the capacitance as possible for cost minimization.

On the other hand, the present invention provides for MIM capacitor which has a greatly increased capacitor density. Furthermore, the present invention is readily

compatible with current semiconductor processing technologies so that CMOS technologies can easily adopt the present invention.

BRIEF SUMMARY OF THE INVENTION

The present invention provides for a high density capacitor structure between adjacent stacked metal layers in an integrated circuit. The metal layers are delineated as interconnections for the integrated circuit. The capacitor structure has a portion of a first selected one of the stacked metal layers and a portion of a second selected one of the stacked metal layers. The second selected stacked metal layer portion is located above and adjacent the first selected stacked metal layer portion. The capacitor structure also has a first capacitor dielectric layer over the first selected stacked metal layer portion; a first capacitor metal plate layer over the first capacitor dielectric layer; a second capacitor dielectric layer under the second selected stacked metal layer portion; a second capacitor metal plate layer under the second capacitor dielectric layer and over and removed from the first capacitor metal plate layer; and a metal capacitor via layer between and connecting said the capacitor metal plate layer and the second capacitor metal plate layer, and a first via connecting the first selected stacked metal layer portion and the second selected stacked metal layer portion. The metal capacitor via layer forms a first terminal of the capacitor structure; and the first via forms a second terminal of the capacitor structure.

The present invention also provides for a method of manufacturing a high density capacitor structure between first and second metallic interconnections of an integrated circuit. The first and second metallic interconnections are separated by an insulating intermetallic oxide layer and the method has the steps of disposing a first metal-dielectric-metal layer capacitor over and with a portion of the first metallic interconnection portion; disposing a second metal-dielectric-metal layer capacitor under and with a portion of the second metallic interconnection; disposing a first metal via through the insulating intermetallic oxide layer to connect the first metal-dielectric-metal layer capacitor and said second metal-dielectric-metal layer capacitor; and disposing a second metal via through the insulating intermetallic oxide layer to connect the first metallic interconnection portion and said second metallic interconnection portion. The first metal via layer forms a first terminal of the capacitor structure and the second metal via form a second terminal of the capacitor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a cross-sectional representational view of a current MIM capacitor structure in an integrated circuit manufactured by conventional interconnection metallization CMOS processes; Fig. 1B is a detailed cross-sectional view of the capacitor structure of Fig. 1A;

Fig. 2 is an electrical circuit representation of the capacitor structure in Fig. 1A;

Fig. 3A is a cross-sectional representational view of another current MIM capacitor structure in an integrated circuit manufactured by damascene interconnection metallization CMOS processes; Fig. 3B is a detailed cross-sectional view of the capacitor structure of Fig. 3A;

Fig. 4A is a cross-sectional representational view of a capacitor structure in an integrated circuit manufactured by damascene interconnection metallization CMOS processes, according to one embodiment of the present invention, Fig. 4B is a detailed cross-sectional view of the capacitor structure of Fig. 4A;

Fig. 5A is an electrical circuit representation of the capacitor structure in Fig. 4A; Fig. 5B is illustrates the electrical circuit representation in Fig. 5A as connected in Fig. 4A;

Figs. 6A-6H illustrate various process steps used in the manufacture of the capacitor structure of Fig. 4A.

DETAILED DESCRIPTION OF THE INVENTION

To illustrate the problem of capacitor density, a capacitor structure in a integrated circuit manufactured by a conventional non-damascene process is shown in Fig. 1A. For purposes of describing the present invention, only the details of the metallization layers forming parts of the capacitor structure are described. Other parts of the integrated circuit are described generally to illustrate the location and problems of the capacitor structure in an integrated circuit. An exemplary six-layer metallization integrated circuit is shown and each metallization layer is labeled M1, for the metallization layer nearest the substrate through M6, the top metallization layer, by terminology common in the semiconductor processing industry.

The exemplary integrated circuit of Fig. 1A is formed on a semiconductor substrate 10 in which active regions 11, such as the source and drain regions of MOS transistors, or substrate conducting regions, are created. To interconnect the regions 11, the

metallization layers M1-M6 are formed over the substrate 10. Each metallization layer is formed by one or more stacked metal layers (represented by only one metal layer in Fig. 1A) which are delineated into interconnecting lines over the top surface of substrate 10. Insulating layers electrically isolate the metallization layers from each other with metal vias through the insulating layers making the electrical contacts between metallization layers at selected locations.

In Fig. 1A, an insulating layer 12 covers the substrate 10 with vias 13 making contact between the active regions 11 and the M1 metal layers 14. An insulating layer 15 covers the M1 metal layers 14 and isolates them from M2 metal layers 17. Vias 16 make the connections between the M1 and M2 metal layers 14, 17. In a similar fashion, an insulating layer 19 covers the M2 metal layers 17 and isolates them from M3 metal layers 20; vias 19 make the connections between the M2 and M3 metal layers 17, 20. An insulating layer 21 covers the M3 metal layers 20 and isolates them from M4 metal layers 23; vias 22 make the connections between the M3 and M4 metal layers 20, 23. An insulating layer 24 covers the M4 metal layers 23 and isolates them from M5 metal layers 26; vias 25 make the connections between the M4 and M5 metal layers 23, 26. An insulating layer 27 covers the M5 metal layers 26 and isolates them from M6 metal layers 30; vias 28 make the connections between the M5 and M6 metal layers 26, 30. Finally, a passivation layer 31 covers the M6 metal layers 30 to protect them physically and electrically from the outside world.

A MIM capacitor structure which is encircled by a dotted line is created between the M5 and M6 layers. The capacitor structure is created by a capacitor dielectric layer 32 on top of a portion of the M5 metal layer 26 and a capacitor metal layer 33 on top of the capacitor dielectric layer 32. Metal vias 29 connect the capacitor metal layer 33 to the M6 metal layer 30. The details of the capacitor structure is shown in greater detail in Fig. 1B. Note that the M5 metal layer 26 is formed by a stacked sandwich of metal layers 26A-26C, as is the capacitor metal layer 33 by a stacked sandwich of metal layers 33A-33C. These stacked sandwich metallic structures are a result of current semiconductor metallization processes. The metal layers 33A-33C are typically TiN/AlCu/TiN; the M5 metal layers 26A-26C are similarly formed with a thicker AlCu layer.

The resulting capacitor structure forms a plate capacitor C with its two terminals in the M5 and M6 metallization layers, as represented in Fig. 2. The density of the capacitor C is determined by the thickness of the capacitor's dielectric layer and the layer's dielectric constant, which places limitations on an increase of the capacitor density. The materials readily available as capacitor dielectric material in CMOS process technology are

typically SiO_2, SiON and SiN, which have relative dielectric constants in a limited range of 4-7. It is tempting to increase the capacitor density by decreasing the thickness of the dielectric layer. However, semiconductor processing limitations, i.e., reliability and thickness control considerations, impose thickness' which are greater than 300Å. Hence even though a MIM capacitor structure can be manufactured from normal metal layers in a straightforward manner in a standard subtractive etch interconnect process, the result is a very low density capacitor. The capacitance structure shown in Fig. 1A has been used to provide capacitance in the range of 1 fF/um^2 (with a dielectric layer having a relative dielectric constant of 4 and a thickness of 350 Å). Hence an increase in the capacitor density in MOS integrated circuits is highly problematical.

Sub A') Nor are the results improved using more modern damascene processes for the metallization layers of the integrated circuit. Fig. 2A illustrates a current MIM capacitor structure in a integrated circuit manufactured by an exemplary damascene process with the advantage of requiring only one additional masking step. Again, only the details of the metallization layers forming parts of the capacitor structure are described and the capacitor structure which is encircled by a dotted line is shown in greater detail in Fig. 2B.

An insulating layer 42 covers a substrate 40 with vias 43 making contact between the active regions 41 and the M1 metal layers 44. An insulating layer 45 covers the M1 metal layers 44 and isolates them from M2 metal layers 47. Vias 46 make the connections between the M1 and M2 metal layers 44, 47. In a similar fashion, an insulating layer 49 covers the M2 metal layers 47 and isolates them from M3 metal layers 50; vias 49 make the connections between the M2 and M3 metal layers 47, 50. An insulating layer 51 covers the M3 metal layers 50 and isolates them from M4 metal layers 53; vias 52 make the connections between the M3 and M4 metal layers 50, 53. An insulating layer 54 covers the M4 metal layers 53 and isolates them from M5 metal layers 56; vias 55 make the connections between the M4 and M5 metal layers 53, 56. An insulating layer 57 covers the M5 metal layers 56 and isolates them from M6 metal layers 60; vias 58 make the connections between the M5 and M6 metal layers 56, 60. Finally, a passivation layer 61 covers the M6 metal layers 60 to protect them physically and electrically from the outside world.

Sub A2 The MIM capacitor structure is created by a capacitor dielectric layer 62 on a portion of the M5 metal layer 56 and a capacitor metal layer 63 on the capacitor dielectric layer 62. A metal via 59 connects the capacitor metal layer 63 to the M6 metal layer 60. The details of the capacitor structure is shown in greater detail in Fig. 1B. Note that the M5 metal layer 56 is formed by a Cu layer 56B surrounded by a Ta layer 56A. The capacitor metal

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layer 63 is a stacked sandwich structure of TiN/AlCu/TiN or Ta/Cu/Ta for the metal layers 63A-63C.

The resulting capacitor structure is still a capacitor between the M5 and M6, as illustrated in Fig. 2. As in the case of capacitor structure of Fig. 1A, the capacitance of the Fig. 3A capacitor structure can only be increased by increasing the area of capacitor plates, i.e., the capacitor portion of the M5 metal layer 56 and the capacitor plate layer 63. As explained above, this results in the undesirable consumption of the integrated circuit's valuable space. A much better result is to increase the capacitor density so that the capacitance of the capacitor structure can be increased without increasing its area.

The present invention provides for just such an increase in capacitor density. Fig. 4A shows a MIM capacitor structure which results in a 2X density improvement over the capacitor structure of Fig. 3A. Only one additional mask step over the interconnect metallization process used in Fig. 3A is required. The disclosed structure is shown in Fig. 4a. The electrical representation of the capacitors obtained is shown in Fig. 5b. With reference to Fig. 4, one terminal of the capacitor is formed at the via metallization and the other terminal is the metal 5/metal 6 which are connected together to give the capacitor shown in Fig. 5b.

In a similar manner as described in the previous drawings, elements 70-86 describe the substrate, active regions, insulating layers, vias and metal layers for the M1 through M5 metallization interconnection layers. An insulating layer 87 separates the M5 metal layer 86 from the M6 metal layer 90 with vias 88 make the connection between the two metal layers 86, 90. Over the M6 metal layer 90 is a passivation layer 96.

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The capacitor structure of which the M5 metal layer 86 is a part is encircled by a dotted line and shown in greater detail in Fig. 4B. A first capacitor dielectric layer 91 is placed on a portion of the M5 metal layer 86 and a first metal capacitor plate layer 92 on the dielectric layer 91. Below a portion of the M6 metal layer 90 above the first capacitor dielectric layer 91 and first metal capacitor plate layer 92 is a second metal capacitor plate layer 95 and a second capacitor dielectric layer 93. A metal via 89 separates (and connects) the first metal capacitor plate layer 91 and the second capacitor dielectric layer 93. Fig. 4A illustrates the composition of some of the elements of the capacitor structure in greater detail. The M5 metal layer 86 is formed by a barrier metal layer 86A of Ta around a Cu metal layer 86B. The first capacitor dielectric layer 91 (and second capacitor dielectric layer 93) is formed by deposited SiO_2, SiON or SiN. The first metal capacitor plate layer 92 (and second metal capacitor plate layer 95) is a tripartite sandwich structure of metal layers 92A-92C (and

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95A-95C) of TiN/AlCu/TiN or Ta/Cu/Ta. The via 89, like the other vias in the metallization interconnection of Fig. 4A is Cu or W.

The MIM capacitor structure forms two capacitors C_1 and C_2 as represented in Fig. 5A. The bottom capacitor C_1 is connected to the M5 metallization layer 86 and the top capacitor C_2 is connected to the M6 metallization layer 90. The via 89, which is actually part of the capacitor structure, connects the two capacitors C_1 and C_2. Structurally it should be noted that in Fig. 4A a right side via 88 connects the M5 metal layer 86 which has a portion covered by the first dielectric layer 91 to the M6 metal layer 90 which has a portion which covers the second metal capacitor plate layer 95. The via 89 connects to M5 and M6 metal layers 86, 90 which are not part of the capacitor structure. To ensure that connection the via 89 is also connected to a via 88 on the left side of the Fig. 4A drawings. Electrically the two capacitors C_1 and C_2 form a circuit shown in Fig. 5B. In other words, if the two capacitors C_1 and C_2 have equal capacitance, the capacitor density is doubled. In the same occupied area, the capacitance is doubled.

The capacitor structure is easily implemented in damascene metallization interconnection processes commonly used in advanced integrated circuits. No new process module developments are required to implement the capacitor disclosed structure.

In a single damascene process, this is demonstrated by Table I which compares M5 metallization through contact pad/etch ally process steps for a standard single damascene process, the same process with a conventional MIM capacitor structure (e.g., Fig. 3A), and the same process with the MIM capacitor structure (e.g., Fig. 4A) according to the present invention.

Std. Damascene Process	With Conventional MIM cap	With Novel MIM Cap
M5 Cu CMP	M5 Cu CMP	M5 Cu CMP
	Deposit metal/insulator stack	Deposit insulator/metal stack
	Pattern and etch MIM cap	Pattern and etch MIM cap
Deposit SiN barrier /IMO layer	Deposit SiN barrier /IMO layer	Deposit SiN barrier /IMO layer
Pattern and etch Via 5	Pattern and etch Via 5	Pattern and etch Via5
Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier
Deposit Cu	Deposit Cu	Deposit Cu
CMP Cu	CMP Cu	CMP Cu
		Deposit insulator/metal stack
		Pattern and etch MIM cap
Deposit SiN barrier /IMOlayer	Deposit SiN barrier /IMOlayer	Deposit SiN barrier /IMOlayer
Pattern and etch trenches for M6 interconnects	Pattern and etch trenches for M6 interconnects	Pattern and etch trenches for M6 interconnects
Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier
Deposit Cu	Deposit Cu	Deposit Cu
CMP Cu	CMP Cu	CMP Cu
Deposit SiN barrier /Passivation	Deposit SiN barrier /Passivation	Deposit SiN barrier /Passivation
Pattern and etch Pad openings	Pattern and etch Pad openings	Pattern and etch Pad openings
Alloy	Alloy	Alloy

Table I

Figs. 6A-6H illustrate some of the process steps in Table I used to manufacture the novel capacitor structure of Fig. 4A with a single damascene process. Fig. 6A illustrates the results after the M5 Cu CMP (Chemical-Mechanical Polishing) step. After metal insulator/insulator stack is deposited over the defined M5 metal layers 86 and insulating layer 84, MIM capacitor pattern and etch steps are performed to define the first capacitor dielectric layer 91 and first capacitor plate layer 92 illustrated in Fig. 6B. The top of the portion of the M5 metal layer 86 is used as the lower metal capacitor plate. (Alternatively, that the capacitor C_1 could be created with a metal insulator/insulator/metal stack deposition steps and followed by MIM capacitor pattern and etch steps to add a separate metal capacitor plate below the dielectric layer 91.) Then an insulating layer 87, formed as a two-layer stack of SiN barrier layer and an IMO (InterMetallic Oxide) layer, is deposited. The apertures, called Via 5 in process table, for the vias 88 and 89 patterned and etched, as shown in Fig. 6C. Then a copper seed or a barrier layer is deposited, which is followed by a copper layer. A CMP process step leaves the metallization as shown in Fig. 6D.

This is followed by capacitor metal insulator/insulator layer stack deposition steps, and the second capacitor dielectric layer 93 and the second capacitor metal plate layer 95 are defined by the MIM pattern and etch steps shown in Fig. 6E. The top of the portion of the via 89 is used as the lower metal capacitor plate. (Again, an alternate embodiment of the capacitor C_2 can be created with a separate metal capacitor plate below the dielectric layer 93 by performing capacitor metal insulator/insulator/metal layer stack deposition steps followed by the MIM pattern and etch steps.) Fig. 6F illustrate the metallization after the insulating layer 94, formed as a two-layer stack of SiN barrier layer and an IMO (InterMetallic Oxide) layer, is deposited and the apertures for the eventual M6 metal layers 90 are patterned and etched. To create the M6 metal layers 90, a copper seed or a barrier layer is deposited, which is followed by a copper layer. A CMP process step for the copper leaves the metallization shown in Fig. 6G. Then the passivation layer 96, actually including a barrier SiN layer also, is deposited. Then passivation layer 96 is pattern and etched for the bonding pads and their connections to the metallization interconnection of the integrated circuit and an aluminum alloy is deposited. Further process steps are required to complete the integrated circuit but are beyond the scope of the present invention.

It should be evident that various materials or combinations of materials can be used for metallization interconnection and the capacitor structure. The dielectric layer for the MIM capacitor structure may be SiO_2 (which can be deposited by a variety of methods, such as PECVD (Plasma-Enhanced Chemical Vapor Deposition), HDP (High Density Plasma), TEOS-Ozone, SACVD (Standard-Atmosphere Chemical Vapor Deposition), etc.), or Silicon-rich SiO_2, SiON, SiN, etc. A variety of metallization stack layers can also be used, such as Cu (with barrier layers of Ta, TiN, TaN, etc.); or AlCu (with barrier layers of TiN). For the metal vias, it is possible to use tungsten (W), besides copper (Cu).

The present invention can also be adapted to dual damascene metallization processes. In a dual damascene process flow, the integration of the new MIM capacitor process (in between, say, the M5 and M6 metallization layers) requires that for those steps, i.e., the Via5 and M6 deposition and definition steps, the dual damascene process be replaced by single damascene process. The process flow changes are shown in Table II, which compares M5 metallization through contact pad/etch ally process steps for a standard dual damascene process, the same process with a conventional MIM capacitor structure (e.g., Fig. 3A), and the same process with the MIM capacitor structure according to the present invention.

Standard Damascene Process	With Conventional MIM cap	With Novel MIM Cap
M5 Cu CMP	M5 Cu CMP	M5 Cu CMP
	Deposit metal/insulator stack	Deposit insulator/metal stack
	Pattern and etch MIM cap	Pattern and etch MIM cap
Deposit SiN barrier /IMOlayer	Deposit SiN barrier /IMOlayer	Deposit SiN barrier /IMOlayer
Pattern and etch Via 5	Pattern and etch Via 5	Pattern and etch Via5
Pattern and etch trenches for M6 interconnects	Pattern and etch trenches for M6 interconnects	Pattern and etch trenches for M6 interconnects
Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier	Deposit Cu seed layer/barrier
Deposit Cu	Deposit Cu	Deposit Cu
CMP Cu	CMP Cu	CMP Cu
		Deposit insulator/metal stack
		Pattern and etch MIM cap
		Deposit SiN barrier /IMOlayer
		Pattern and etch trenches for M6 interconnects
		Deposit Cu seed layer/barrier
		Deposit Cu
		CMP Cu
Deposit SiN barrier /Passivation	Deposit SiN barrier /Passivation	Deposit SiN barrier /Passivation
Pattern and etch Pad openings	Pattern and etch Pad openings	Pattern and etch Pad openings
Alloy	Alloy	Alloy

Table II

As can be seen from Tables I and II, the present invention's MIM capacitor structure is highly suitable for a single damascene process. Even in a dual damascene process, the present invention is attractive since all the previous metallization layers M1 through M5 can still be processed with dual damascene steps. In integrated circuits with a large MIM capacitor area, there is still a considerable area and cost savings with the MIM capacitor structure of the present invention.

Therefore, while the description above provides a full and complete disclosure of the preferred embodiments of the present invention, various modifications, alternate constructions, and equivalents will be obvious to those with skill in the art. For example, though the capacitor structure of the present invention has been described as being located between the M5 and M6 metallization layers, it should be understood that other metallization layers can be used also. Thus, the scope of the present invention is limited solely by the metes and bounds of the appended claims.